1. INTRODUCTION

The Internet as widespread packet data network enables IP Telephony in the form of client software running on multimedia PC for low-cost PC-to-PC communication, but the Quality of Service (QOS) is poor related to QOS of PSTN.

Dramatic growth of Internet and the cellular extension growth of Telephone Network are the challenge to interconnect these two distinct networks in order to obtain more economic utilization of network resources [1].

The VoIP Gateway is this interface unit that enables real-time voice traffic over the IP-based data networks with the suitable QOS.

This paper presents one approach to VoIP Gateway realization in the developing area of voice/data convergence. The suggested solution is given by the functional description of hardware and software modules distributed to the host processor and DSP.

The main target areas of VoIP Gateway are Internet Service Providers that intend to provide voice services with cost reduction in relation to PSTN and the Intranet Business Networks that are urged on reduction the cost of their intercontinental calls.

2. HARDWARE ARCHITECTURE

The hardware of the VoIP Gateway that has been suggested by this paper is presented in Fig. 1.
As the Master Control Unit the MPC860 Motorola 32-bit RISC processor is selected, that integrates communication processor, 4 serial communication controllers, 4 general purpose timers, 4K instruction cache, 4K data cache, system interface unit, PCMCIA controller and power management, having 52.8 MIPS performance at 40 MHz [2]. One serial communication controller is programmed as Ethernet/IEEE 802.3 controller and connected to the MK68592 Serial Interface Adapter, for the interface to the IP network.

Digital Signal Processor DSP56311, Am27C40 EPROM and KM416S1120D DRAM are connected to the MPC860 address and data bus through fast address buffers and data transceivers.

The Am27C40 is AMD 512K x 8 CMOS UV erasable EPROM with access time less than 90ns, and 5V supply with static standby mode [3], used for storing VoIP Gateway master control program modules. The KM416S1120D is Samsung 2 x 512 x 16 synchronous high data rate Dynamic RAM with the range of operating frequencies of 100-183 MHz [4], used to store VoIP Gateway communication data. Synchronous design allows I/O transactions on every clock cycle, enabling burst data read and write.

For the voice processing Motorola DSP56311 digital signal processor is adopted, having 24 x 24 bit parallel multiplier-accumulator, internal 48K x 24 Xdata and Ydata RAM, two Enhanced Synchronous Serial Interface (ESSI) ports, and Host Interface Port [5]. The Host Interface is 8-bit address, 8-bit data bus connected to the MPC860, performing tightly coupled two-processor architecture. The DSP56311 has its own external EPROM Am27V40 and DRAM KM416S1120D memory for store the voice processing program and communication data respectively. Two ESSI, as full duplex serial ports, programmed in network mode for the interface to the time division multiplexed (TDM) signals, are connected to the MH89790 2Mbps PCM circuit, that provide VoIP Gateway Interface to the Public Switched Telephone Network (PSTN).

The MH89790 is Mitel PCM 30 Digital Trunk Interface Circuit, supporting HD3B and AMI line codes, 32 x 64 kbps channels per frame, CRC-4 control in the first channel per frame, multiframe synchronization in the first channel of odd frames, signaling transfer the 16th time channel, and the data transfer in the other 30 eight-bit channels [6]. The MT8940 is Mitel digital PLL circuit [6] locked at the 8KHz signal extracted by the MH89790 circuit from the receiving PCM line, that provides 2MHz clock and frame synchronization for the ESSI ports of DSP56311 processor.

The MK68592 SGS-Thompson Serial Interface Adapter containing Manchester Encoder/Decoder, noise filter and collision detector enables MAC layer interface to Ethernet cable [7]. It is connected to the SCC1 port of MPC860 processor that is programmed to perform the function of Ethernet controller, enabling the VoIP Gateway Interface to the Internet network.

The presented two-processor hardware architecture, adopted after the proper design consideration, can support all requirements of VoIP Gateway.

3. SOFTWARE SUPPORT DESCRIPTION

The VoIP Gateway software is distributed to the Master Control Unit (MCU) software and DSP software, communicating through tightly coupled handshake hardware by means Real Time Protocol packets. System software and Call Processing Software is allocated to the Am27C40 external EPROM of the MPC860 (MCU), while the Voice Processing Software is installed in the Am27C40 EPROM of DSP56311 processor. The data flow diagram of software is presented in Fig. 2. The MPC860 software consists of System Software, Ethernet Controller Support Module, Network Protocol Module, VoIP Application Protocol Module, Address Translation Module and DSP Interface Module. System Software encloses Real Time Operating System (RTOS), Startup Routine, Initialization Routine and Management Functions. Ethernet Controller Module supporting buffer management structure in external DRAM memory of MPC860 MCU provides transference UDP/IP [8] [9] voice packets to the IP network.

Network Protocol Module performs the removing the UDP and IP headers from the incoming voice and signaling packets, and adding these headers to the Real Time Protocol (RTP) packets [10] for sending to the IP network. The VoIP Application Protocol Module converts H.323 packet network signaling protocol [11] into standard CAS line telephony signaling at the packets received from the IP network, and performs the reverse conversion at the packets coming from the telephone network.

Address Translation Module of MCU software performs MF telephony address signaling conversion to the corresponding IP address in the direction of packet transfer to the IP network, and the reverse translation in the opposite direction. The DSP Interface Module supports the RTP packet communication of MPC860 processor with DSP56311, that is memory mapped in its address space.

The Voice Processing Software assigned to DSP56311 Digital Signal Processor consists of PCM Interface Module, Echo Cancel Module, Voice Activity Detection Module, Voice Codec Module, Signaling Tone Detect Module, RTP Packet Protocol Module and Voice Playout Module (Fig. 2).
PCM Interface Module performs the support to the MH89790 circuit providing the VoIP Gateway interface to the PSTN network. PCM frames from the PCM Interface Module arrive to the Echo Cancel Module, that performs echo compensation removing echo delay that produce voice QOS degradation. Voice Activity Detection Module detects incoming voice PCM stream and transfers it to the Voice Codec Module. Signaling Tone Detect Module detects the reception of MF address tones of telephone signaling, and transfers them to the RTP Packet Protocol Module.

Voice Codec Module compresses the voice frames for transmission over the IP network, applying G.729 CS-ACELP standard with the compression ratio 8:1 (64Kbps: 8Kbps), and sends them to the RTP Packet Protocol Module. In the direction to the PSTN network the frames are decompressed from 8Kbps streams to 64Kbps streams.

In RTP Packet Protocol Module several frames are combined in a single packet and the RTP header is added to the packet for the transfer the packet to the IP network. The RTP header provides the packet sequence number and time stamp that enable proper assembling of voice packets at the receiving end. RTP voice and signaling packets are transferred through the DSP Host Interface Port to the MCU software.

Voice Playout Module stores the RTP voice packets received from MCU host processor software into the Jitter Buffer in external DSP DRAM memory, and removes timing jitter from the incoming packet sequence, providing temporal integrity of voice. The RTP Packet Protocol Module removes the RTP header from the incoming packets, performs compensation for network delay, jitter and dropped packets and sends voice frames to the Voice Codec Module.

The Voice Codec Module decompresses G.729 8Kbps frames to the 64Kbps frames sending them to the PCM Interface Module, forming the PCM voice stream for the PSTN network.

Taking care of the factors that affect the voice quality such as minimizing the effects of network delay and jitter, performing echo cancelation and lost packet compensation, the presented VoIP Gateway hardware and software solution approach provides a method of integrating IP networks and PSTN networks with satisfactory voice QOS.

4. CONCLUSION

This paper has presented one approach to a VoIP Gateway realization with system design consideration that has been undertaken. The VoIP
Gateway is based on the closely coupled MPC860 processor and 56311 DSP offering 150 MIPS performance, arranged in a hierarchical fashion with the MPC860 as master control unit and DSP as slave, with their own EPROM and RAM memories. The interface to the Ethernet is acquired through one MPC860’s Serial Communication Port programmed as Ethernet Controller and the MK68592 Serial Interface Adapter, while the connection to the E1 line is anticipated through DSP56311 and MH89790 PCM Interface Circuit.

Software architecture is distributed: system software, call processing and network protocol software is assigned to the MPC860 processor, while the voice processing software is assigned to the DSP56311.

The main factors affecting the QOS of Voice over Internet communication: echo, jitter and packet loss are compensated by the presented Gateway solution. Echo is compensated through line digital filter and Echo Canceller Module in DSP software, jitter by the buffers in Voice Playout Unit Module in DSP software, and packet loss through protocol compensation schemes such as replaying the last received packet and redundant packet sending.

Taking care of all these factors that act on system performance, the QOS at least equal to PSTN is fulfilled by this VoIP Gateway solution approach, what is the main development challenge.

5. REFERENCES


Abstract: This paper has presented one VoIP Gateway Realization Approach. Two-processor architecture with MPC860 as Master Control Unit supporting MK68592 Interface to the IP Network, and DSP56311 as slave, supporting MH89790 E1 Digital Interface to PSTN Network, is considered. Distributed software assigned to the MPC860 processor and DSP56311 is described at module level. Taking care of factors affecting the voice quality, the presented VoIP solution approach enables the QOS at least equal to PSTN.

ONE APPROACH TO VoIP GATEWAY REALIZATION.
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